Amendments to Drawings

The attached sheet of drawings include changes to FIGS. 1 and 3. This sheet, which includes FIGS. 1 and 3, replaces the original sheet including FIGS. 1 and 3.

Attachments:

Replacement Sheet including FIG. 1 and 3

Remarks

Claims 1-2 and 4-14 are pending in the application and are presented for reconsideration. Claims 1, 5-14 have been amended; Claim 3 has been canceled; and Claims 2 and 4 remain in the application unchanged. No new matter has been added.

Support for the amendments to the claims may be found in the specification at least at page 8, lines 19-22 and page 11, line 32 through page 11, line 16.

Drawings

The drawings are objected to as failing to comply with 37 C.F.R. § 1.84(o) because features represented by boxes in the figures must be labeled with a term which indicates what element the box represents.

FIGS. 1 and 3 have been amended to include labels in the boxes to indicate the function that the corresponding box represents.

Applicant respectfully submits that the objections to the drawings are now overcome.

Claim Objections

Claim 1 is objected to because the term "said test data" lacks antecedent basis. Claim 1 has been amended to correct the antecedent basis problem. The Applicant respectfully submits that the objections to the claims are now overcome.

Claim Rejections

Claims 8 and 9 are rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Reis et al. (U.S. Pat. 6,807,644, Reis hereinafter).

The Examiner's rejections of the claims are respectfully traversed.

I. Rejection of Claims Under 35 U.S.C. § 112, Second Paragraph

Claims 8 and 9 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner states that in Claim 8 at line 2, the term "said wireless interface" is unclear. Claim 7 has been amended to distinguish between a "test station wireless interface" and "wireless interfaces of each of the plurality of integrated circuits". The Applicant respectively submits that the language of claims 7-9 now clearly distinguishes between the wireless interface of the test station and the respective wireless interfaces of the integrated circuit devices under test. The Applicant respectfully submits that the rejection of Claim 8 and 9 under 35 U.S.C. § 112, second paragraph are now overcome.

II. Rejections of Claims Under 35 U.S.C. § 103

a. Claims 1-2 and 4-6

Applicant's amended **Claim 1** recites:

> An integrated circuit comprising:
> one or more functional blocks to be tested when said integrated circuit is placed in a test mode;
> one or more test structures configured to test said one or more functional blocks when said integrated circuit is placed in said test mode;
> a wireless interface which receives test data over a wireless connection, the test data comprising a frame having a plurality of bits; and
> a test access mechanism which controls input of said received test data to said test structures, wherein at least two of said plurality of bits of the frame are applied to different respective test structures on said integrated circuit.

The Reis Reference

The Examiner cites Reisi as anticipating claim 1. In particular, the Examiner states that Reis teaches (figures 2, 5 & 7) that a downlink transceivers (TR2), which arrange the signals to be transmitted to an asynchronous transmission path (

ATP), is connected to the side of the transmission path of the test access ports

(TAP) of the device under test (DUT), wherein the asynchronous transmittion path may be wireless. The Examiner further states that Reis further teaches the downlink transceiver (500) (TR2) generates TDI signals from received TMS-TDI packets, and forwards the test data output TDO obtained from the output of boundary scan cell chain of the DUT to the transmission path (figure 2, 5 & 7, column 3 line 52-column 4 line 15, column 5 lines 43-51). The Examiner states that Reis does not explicitly teach a functional block, but that Reis teaches (figure 7) that each of the JTAG compatible circuits (U1 & U2) (in the DUT) comprises a JTAG controller C and the boundary scan register of 27 boundary scan cells BSC (column 6, lines 51-56).

Claim 1 has been amended to recite the limitations "the test data comprising a frame having a plurality of bits" and "a test access mechanism which controls input of said received test data to said test structures, wherein at least two of said plurality of bits of the frame are applied to different respective test structures on said integrated circuit". Reis does not teach or suggest the limitation "wherein at least two of said plurality of bits of the frame are applied to different respective test structures on said integrated circuit". Reis teaches two JTAG compatible circuits U1 & U2, which both comprise a JTAG controller C and the boundary scan register with twenty-seven boundary scan cells BSC. (Reis, column 6, lines 53-56). These circuits U1 & U2 have their boundary scan registers connected in series, such that the output of the boundary scan register of U1 is connected to the input of the boundary scan register of U2. Thus, only one bit is input to only one test structure at a time - i.e., test data is serially input to the boundary scan register of U1 only (and shifted through the boundary scan register of U1 followed by U2).

In contrast, Applicant's Claim 1 recites that "*at least two* of the plurality of bits of the frame are applied to *different* respective test structures on said integrated circuit". Thus, given one frame of test data received over the wireless connection, at least two of the bits in the frame are applied to different test structures. Reis does not teach or suggest this limitation. Furthermore, even if, per the Examiner's suggestion, it would be a matter of design choice for either

serially testing all BSCs in both of the circuits (U1 & U2) or connecting the TAP to a BSC of each of the circuits (U1 & U2), the modification still would not meet the distinguishing limitation of Applicant's Claim 1 because Reis does not teach or suggest the application of different bits of a test data frame to different test structures. Instead, Reis teaches only the serial application of test data to any given BSC. Accordingly, Reis does not meet the limitations of Applicant's Claim 1.

Since Reis, even in combination with the ordinary skill in the art at the time of the invention, does not meet each and every limitation of Applicant's claim 1, Reis cannot be used in formulating an obviousness rejection under 35 U.S.C. § 103.

Claims 2 and 4-6 each depend from independent base claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 2-10 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 2-10 should be withdrawn.

b. Claims 7-12

Claim 7 recites:

> A system for testing an integrated circuit, comprising:
> a plurality of integrated circuits, each comprising:
> one or more functional blocks to be tested when said integrated circuit is placed in a test mode;
> one or more test structures configured to test said one or more functional blocks when said integrated circuit is placed in said test mode;
> a wireless interface which receives and extracts test data from a wireless connection; and
> a test access mechanism which controls input of said received test data to said test structures; and
> a test station comprising a test station wireless interface which simultaneously transmits the test data over the wireless connection to the wireless interfaces of each of the plurality of integrated circuits.

Claim 7 recites "a test station comprising a test station wireless interface which *simultaneously transmits the test data over the wireless connection to the wireless interfaces of each of the plurality of integrated circuits*". Reis does not teach or suggest a plurality of integrated circuits. Reis also does not teach or

suggest a test station that simultaneously transmits test data to more than one integrated circuit. Accordingly, Reis, even in combination with the prior art, does not meet each and every limitation of Applicant's Claim 7.

Since Reis, even in combination with the ordinary skill in the art at the time of the invention, does not meet each and every limitation of Applicant's Claim 7, Reis cannot be used in formulating an obviousness rejection of Claim 7 under 35 U.S.C. § 103.

Claims 8-12 each depend from independent base Claim 7 and add further limitations. For at least the same reasons that Claim 7 is not shown, taught, or disclosed by the cited references, Claims 8-12 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 8-12 should be withdrawn.

b. Claims 13-14

Claim 13 recites:

> A method for testing integrated circuits, comprising:
> obtaining test data;
> simultaneously sending said test data via a wireless interface over a wireless connection to a plurality of integrated circuit devices under test, each comprising one or more functional blocks to be tested when said respective integrated circuit device under test is placed in a test mode, one or more test structures configured to test said one or more functional blocks when said respective integrated circuit device under test is placed in said test mode, a wireless interface which receives and extracts said test data from said wireless connection; and a test access mechanism which controls input of said received test data to said test structures of said respective integrated circuit device under test.

Claim 13 recites similar limitations as Claim 7, including "simultaneously sending said test data via a wireless interface over a wireless connection to a plurality of integrated circuit devices under test". For at least the same reasons that Claim 7 is not shown, taught, or disclosed by the cited references, Claim 13 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 13 should be withdrawn.

Claim 14 each depend from independent base Claim 13 and add further limitations. For at least the same reasons that Claim 13 is not shown, taught, or

disclosed by the cited references, Claim 14 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 14 should be withdrawn.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-2 and 4-14 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

August 18, 2006

Jessica Costa

Jessica Costa, Reg. No. 41,065

The Law Offices of Jessica Costa, PC
P.O. Box 460 Crozet, VA
22932-0460
(434) 823-2232
(434) 823-2242 (fax)